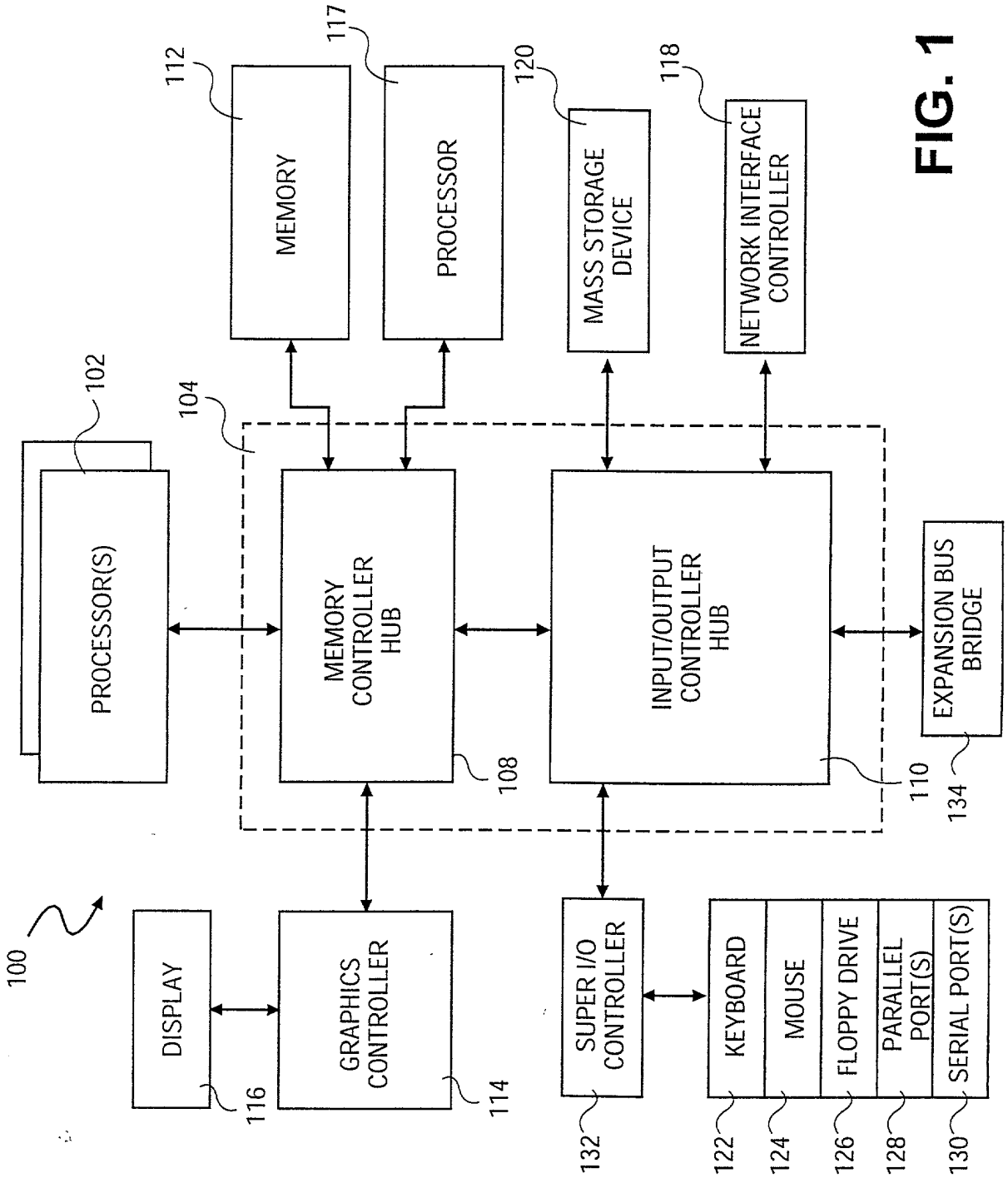
100
PROCESSOR(S)
102
MEMORY CONTROLLER HUB
104
108
INPUT/OUTPUT CONTROLLER HUB
110
EXPANSION BUS BRIDGE
134
MEMORY
112
PROCESSOR
117
MASS STORAGE DEVICE
120
NETWORK INTERFACE CONTROLLER
118
DISPLAY
116
GRAPHICS CONTROLLER
114
SUPER I/O CONTROLLER
132
KEYBOARD
122
MOUSE
124
FLOPPY DRIVE
126
PARALLEL PORT(S)
128
SERIAL PORT(S)
130

FIG. 1

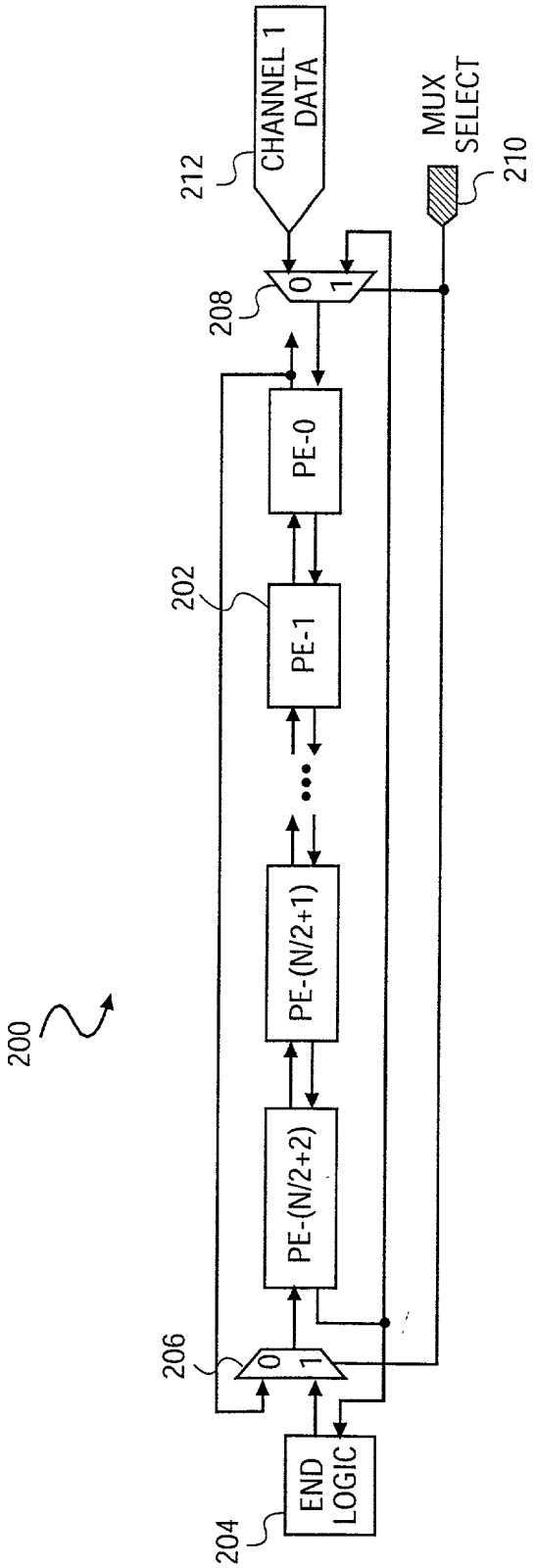
200
CHANNEL 1 DATA
212
MUX SELECT
210
208
0
1
PE-0
202
PE-1
PE-(N/2+1)
PE-(N/2+2)
206
0
1
END LOGIC
204

FIG. 2

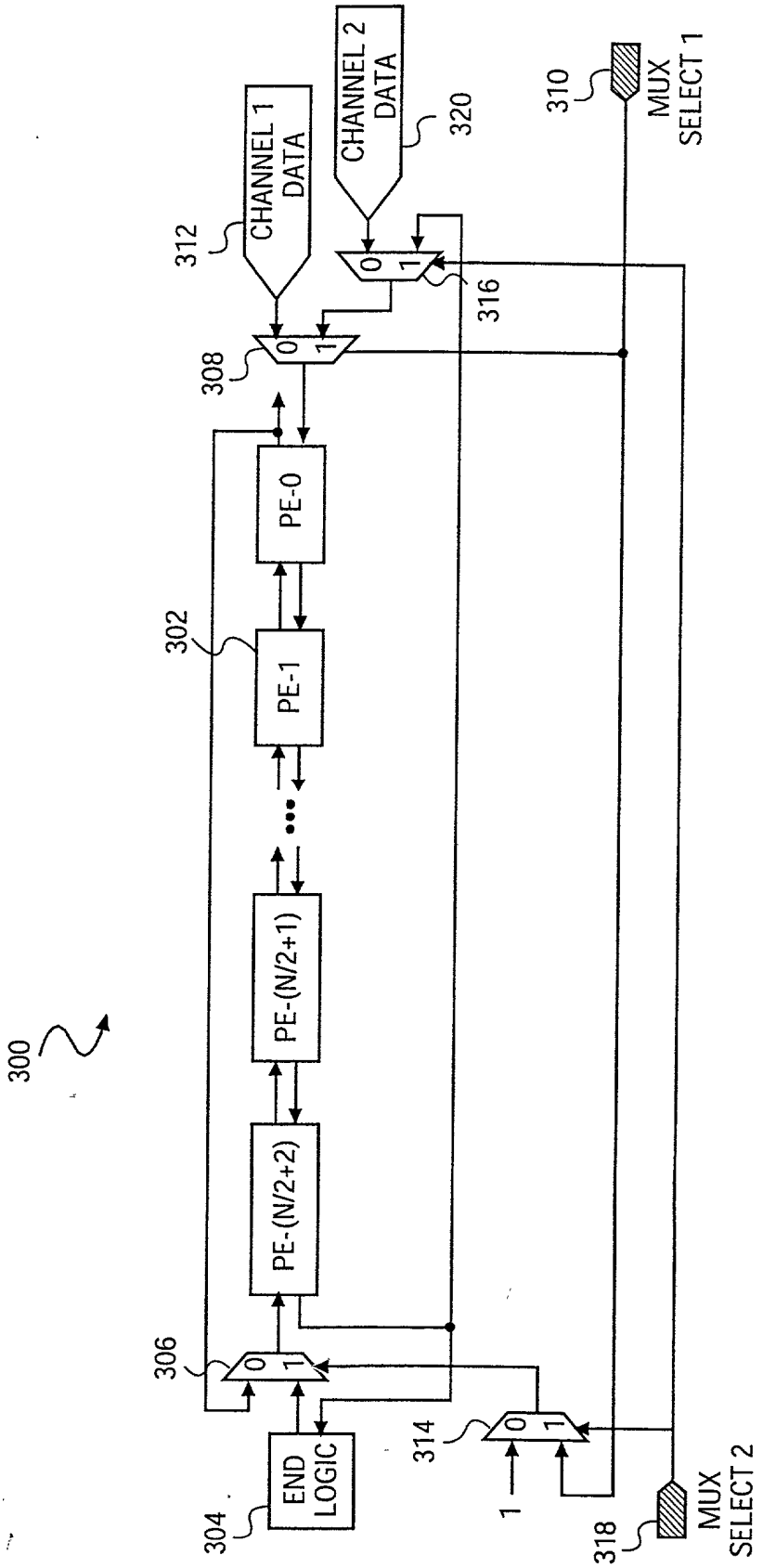
300
CHANNEL 1 DATA
312
CHANNEL 2 DATA
320
310
MUX SELECT 1
316
308
PE-0
302
PE-1
PE-(N/2+1)
PE-(N/2+2)
306
END LOGIC
304
314
1
318
MUX SELECT 2

FIG. 3

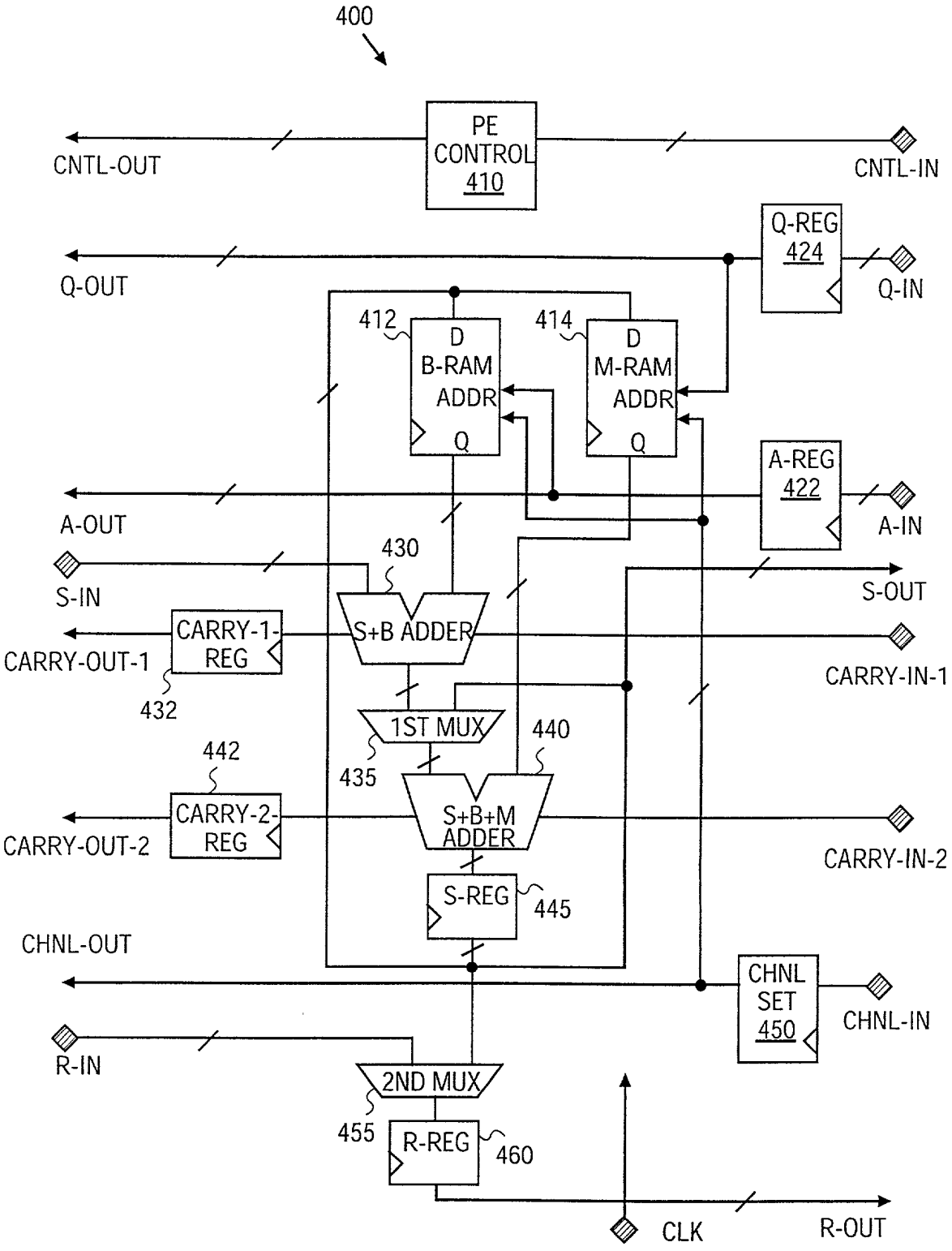
400
PE CONTROL 410
CNTL-OUT
CNTL-IN
Q-REG 424
Q-OUT
Q-IN
412
D B-RAM ADDR Q
414
D M-RAM ADDR Q
A-REG 422
A-OUT
A-IN
430
S-IN
S-OUT
CARRY-1-REG
S+B ADDER
CARRY-OUT-1
CARRY-IN-1
432
1ST MUX
435
440
442
CARRY-2-REG
S+B+M ADDER
CARRY-OUT-2
CARRY-IN-2
S-REG
445
CHNL-OUT
CHNL SET 450
CHNL-IN
R-IN
2ND MUX
455
R-REG
460
CLK
R-OUT

FIG. 4

CYCLE	MUX SELECT	END LOGIC	PE-6	PE-5	PE-4	PE-3	PE-2	PE-1	PE-0	INPUT REGS
1	0								0	
2	1							1		
3	0						2		0	
4	1					3		1		
5	0				4		2		0	
6	1			5		3		1		
7	0		6		4		2		0	
8	1			5		3		1	7	
9	0		6		4		2	8	0	
10	1			5		3	9	1	7	
11	0		6		4	10	2	8	0	
12	1			5	11	3	9	1	7	
13	0		6	12	4	10	2	8	0	
14	1		13	5	11	3	9	1	7	
15	0		6	12	4	10	2	8	0	
16	1		13	5	11	3	9	1	7	
17	0		6	12	4	10	2	8	0	
18	1		13	5	11	3	9	1	7	
19	0		6	12	4	10	2	8	0	
20	1		13	5	11	3	9	1	7	

FIG. 5

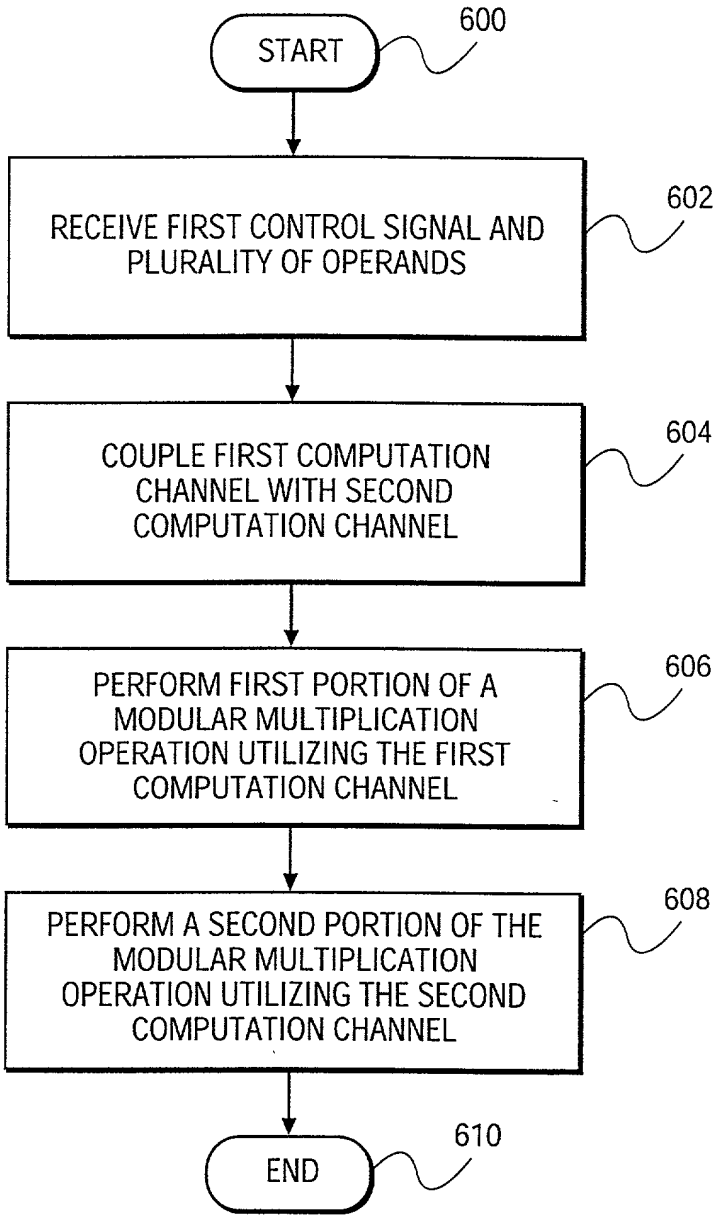
START
600
RECEIVE FIRST CONTROL SIGNAL AND PLURALITY OF OPERANDS
602
COUPLE FIRST COMPUTATION CHANNEL WITH SECOND COMPUTATION CHANNEL
604
PERFORM FIRST PORTION OF A MODULAR MULTIPLICATION OPERATION UTILIZING THE FIRST COMPUTATION CHANNEL
606
PERFORM A SECOND PORTION OF THE MODULAR MULTIPLICATION OPERATION UTILIZING THE SECOND COMPUTATION CHANNEL
608
END
610

FIG. 6